

Abstract

A method of a modeling metallization parasitics with the use of a simulation program. In one embodiment, a method of simulating interconnect lines in an electronic design automation simulation is disclosed. The method comprises partitioning the interconnect lines into groups of interconnect lines. Each group of interconnect lines does not have interactions with any of the other groups of interconnect lines. Moreover, at least one of the groups of interconnect lines contains at least three interconnect lines. The interconnect lines in each group are modeled. The modeling includes at least one of modeling mutual inductances and modeling of mutual capacitances.